

FIG. 1

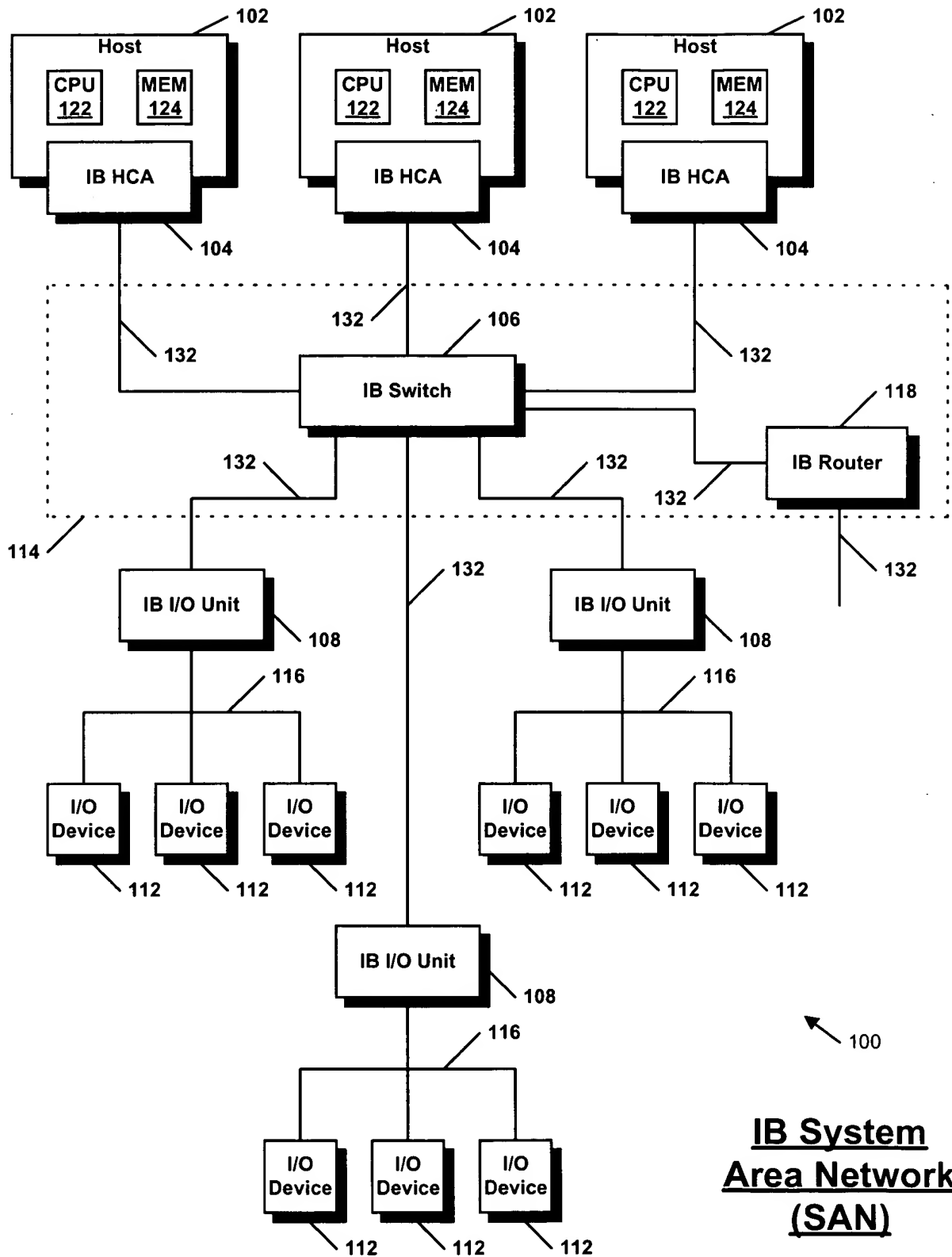
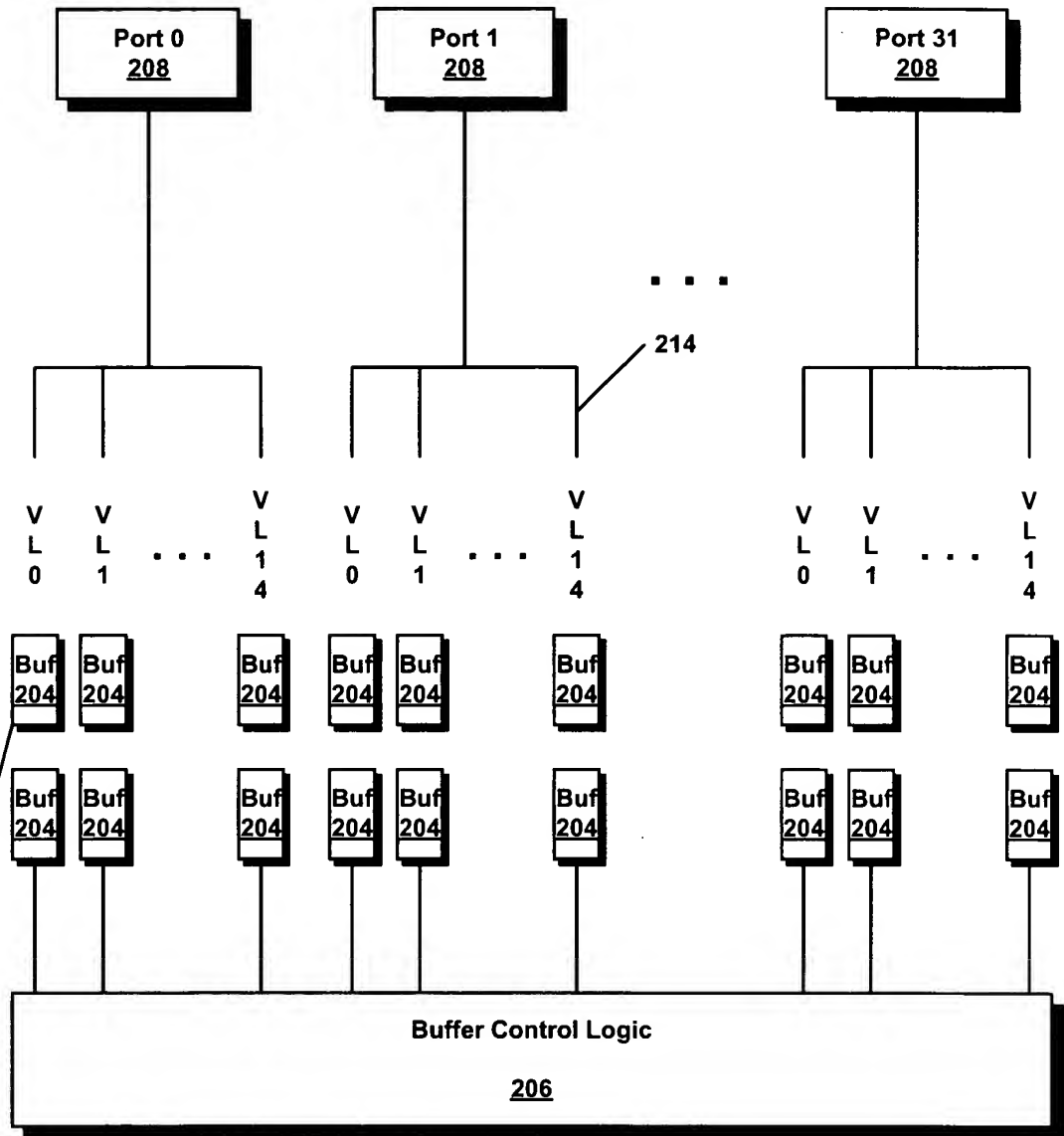


FIG. 2 (Related Art)

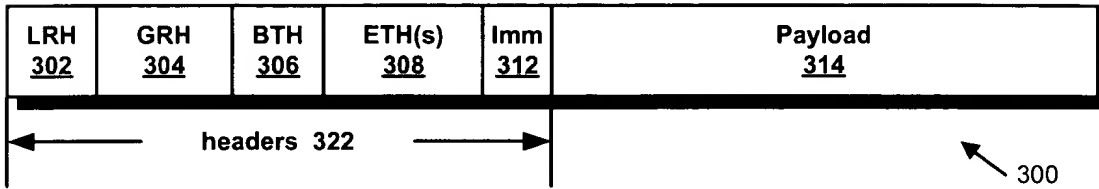


two
maximum IB
packet-sized
(4224 byte)
buffers
dedicated
per port/VL

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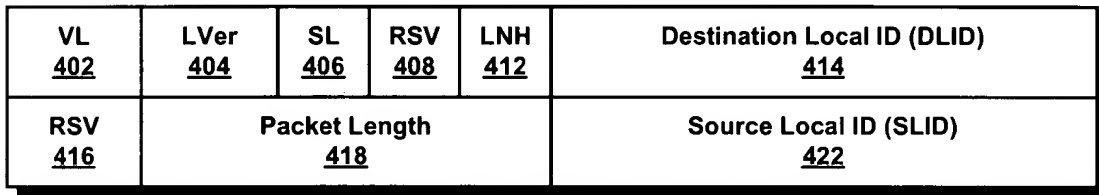
Conventional IB Switch

FIG. 3 (Related Art)



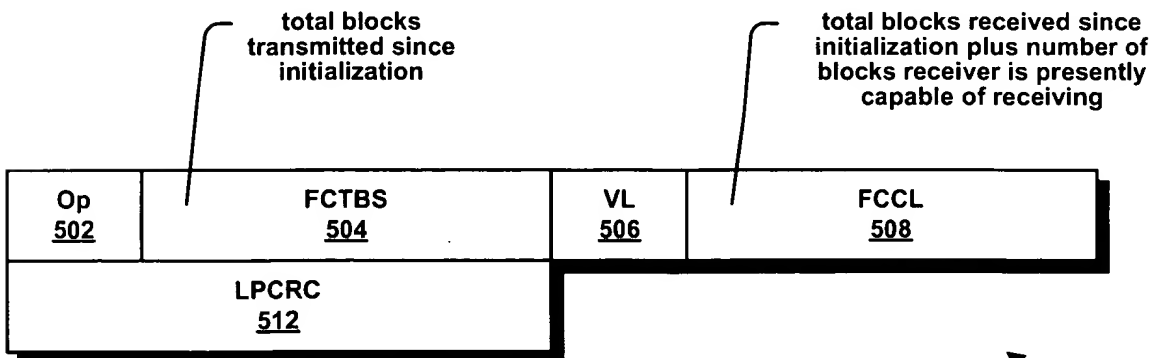
IB Data Packet

FIG. 4 (Related Art)



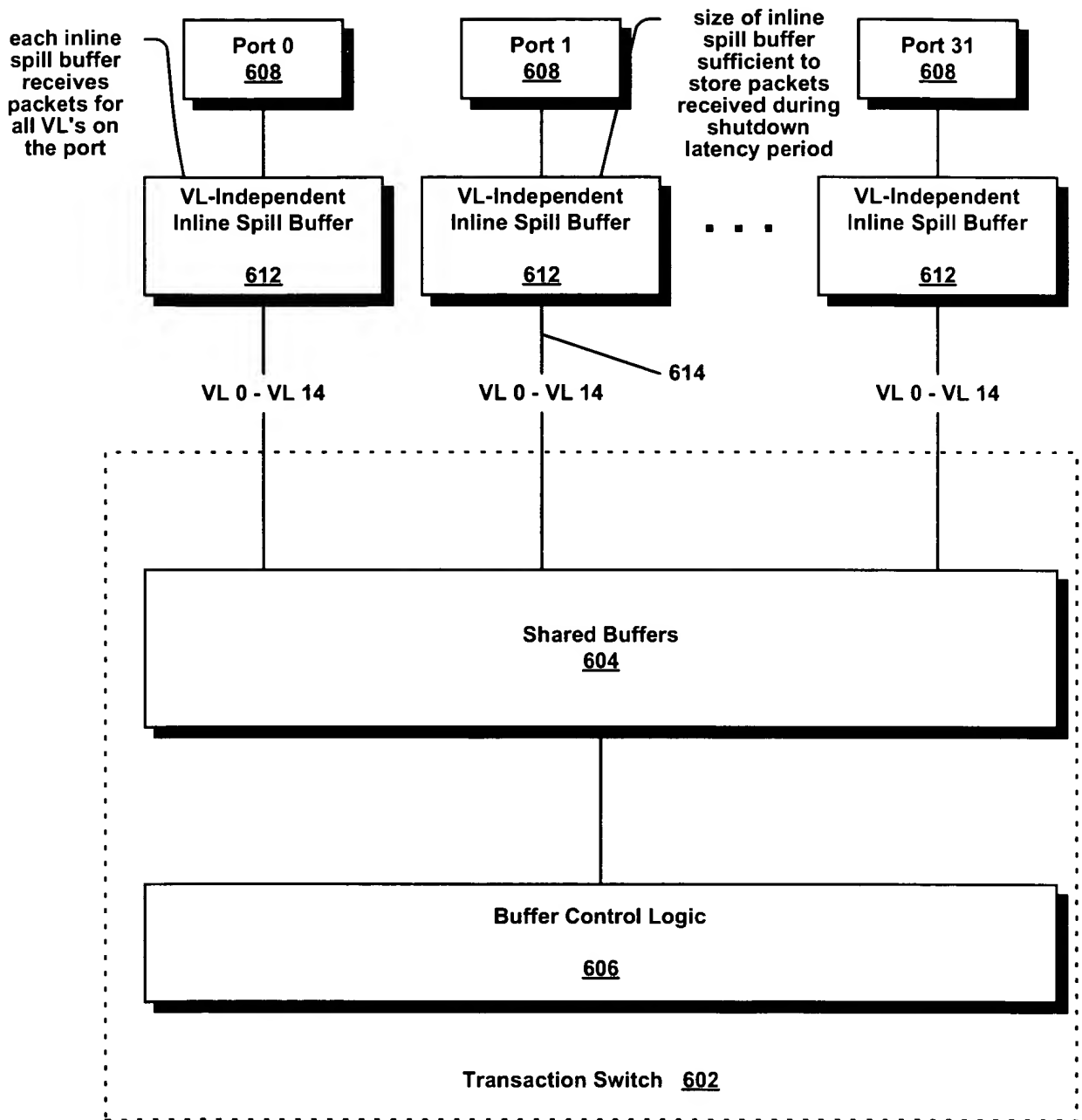
Local Routing Header

FIG. 5 (Related Art)



Flow Control Packet

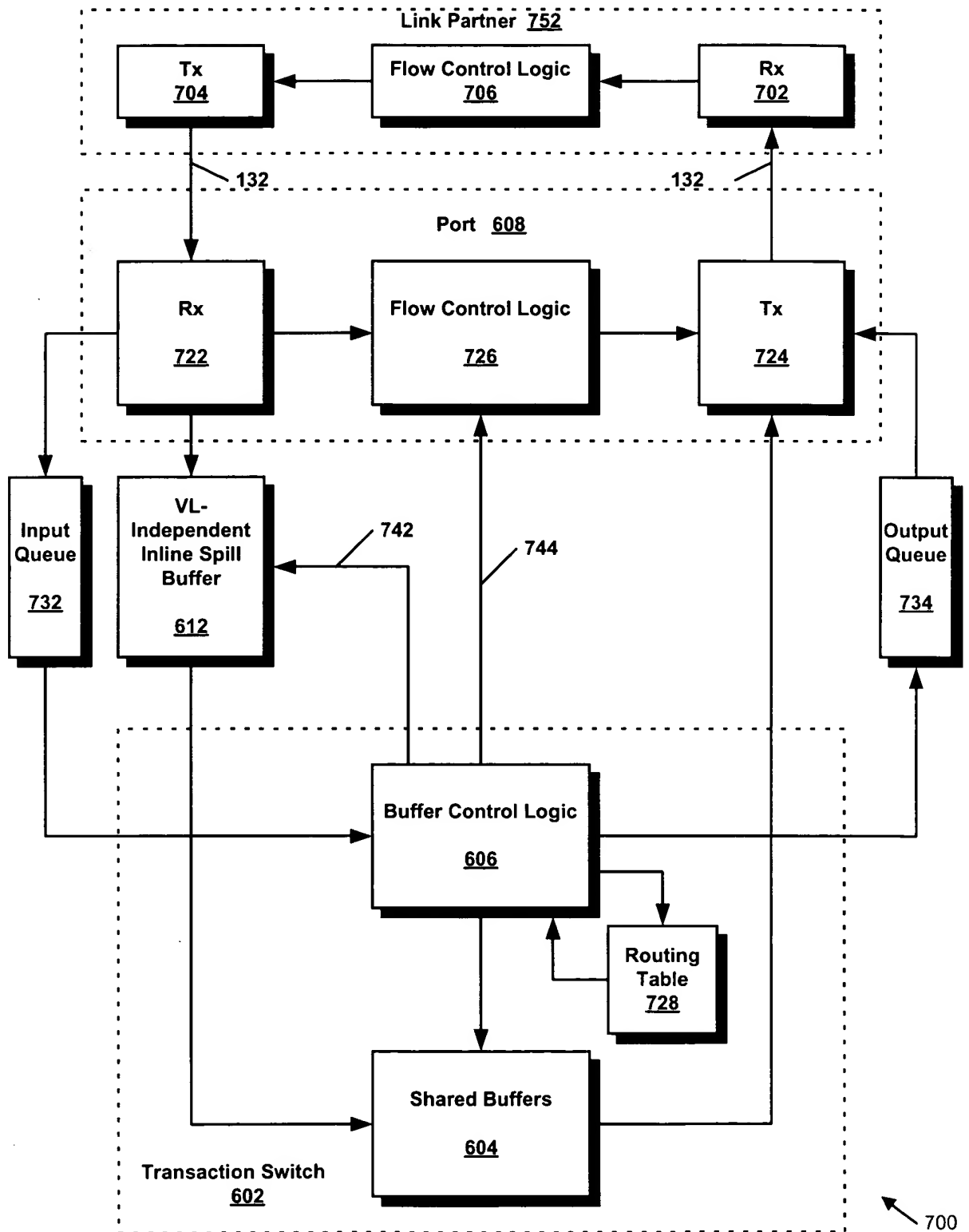
FIG. 6



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IB Switch Capable of Over-Advertising Buffering Resources Using Inline Spill Buffer

FIG. 7



Packet Buffering System Using Inline Spill Buffer

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Valid	Good Packet	VL	GRH present	DLID	SLID	Packet Length	Destination QP
<u>802</u>	<u>804</u>	<u>806</u>	<u>808</u>	<u>812</u>	<u>814</u>	<u>816</u>	<u>818</u>

Input Queue Entry

800

FIG. 9

Tag	VL	Packet Length	Chunk Address 0	Chunk Address 1	Chunk Address 2	Chunk Address 3	Chunk Address 4	Chunk Address 5
<u>902</u>	<u>904</u>	<u>906</u>	<u>908</u>	<u>912</u>	<u>914</u>	<u>916</u>	<u>918</u>	<u>922</u>

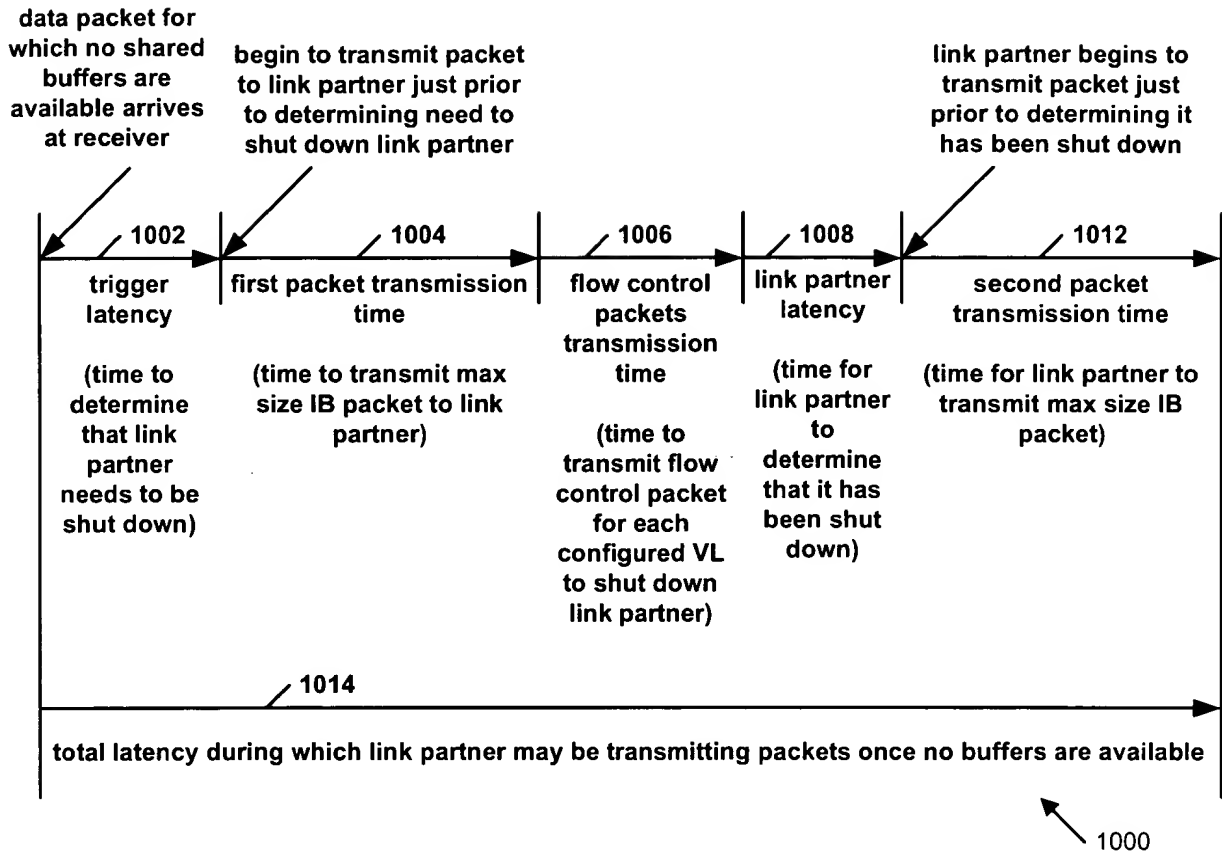
Output Queue Entry

900

Wavelength, μ	Wavelength, μ	Wavelength, μ	Wavelength, μ	Wavelength, μ	Wavelength, μ
0.405	0.436	0.480	0.546	0.630	0.708
0.845	0.900	1.014	1.108	1.250	1.380
1.550	1.650	1.875	2.140	2.486	2.850
3.250	3.650	4.050	4.450	4.850	5.250
5.650	6.050	6.450	6.850	7.250	7.650
8.050	8.450	8.850	9.250	9.650	10.050
10.450	10.850	11.250	11.650	12.050	12.450
12.850	13.250	13.650	14.050	14.450	14.850
15.250	15.650	16.050	16.450	16.850	17.250
17.650	18.050	18.450	18.850	19.250	19.650
20.050	20.450	20.850	21.250	21.650	22.050
22.450	22.850	23.250	23.650	24.050	24.450
24.850	25.250	25.650	26.050	26.450	26.850
27.250	27.650	28.050	28.450	28.850	29.250
29.650	30.050	30.450	30.850	31.250	31.650
32.050	32.450	32.850	33.250	33.650	34.050
34.450	34.850	35.250	35.650	36.050	36.450
36.850	37.250	37.650	38.050	38.450	38.850
39.250	39.650	40.050	40.450	40.850	41.250
41.650	42.050	42.450	42.850	43.250	43.650
44.050	44.450	44.850	45.250	45.650	46.050
46.450	46.850	47.250	47.650	48.050	48.450
48.850	49.250	49.650	50.050	50.450	50.850
51.250	51.650	52.050	52.450	52.850	53.250
53.650	54.050	54.450	54.850	55.250	55.650
56.050	56.450	56.850	57.250	57.650	58.050
58.450	58.850	59.250	59.650	60.050	60.450
60.850	61.250	61.650	62.050	62.450	62.850
63.250	63.650	64.050	64.450	64.850	65.250
65.650	66.050	66.450	66.850	67.250	67.650
68.050	68.450	68.850	69.250	69.650	70.050
70.450	70.850	71.250	71.650	72.050	72.450
72.850	73.250	73.650	74.050	74.450	74.850
75.250	75.650	76.050	76.450	76.850	77.250
77.650	78.050	78.450	78.850	79.250	79.650
80.050	80.450	80.850	81.250	81.650	82.050
82.450	82.850	83.250	83.650	84.050	84.450
84.850	85.250	85.650	86.050	86.450	86.850
87.250	87.650	88.050	88.450	88.850	89.250
89.650	90.050	90.450	90.850	91.250	91.650
92.050	92.450	92.850	93.250	93.650	94.050
94.450	94.850	95.250	95.650	96.050	96.450
96.850	97.250	97.650	98.050	98.450	98.850
99.250	99.650	100.050	100.450	100.850	101.250
101.650	102.050	102.450	102.850	103.250	103.650
104.050	104.450	104.850	105.250	105.650	106.050
106.450	106.850	107.250	107.650	108.050	108.450
108.850	109.250	109.650	110.050	110.450	110.850
111.250	111.650	112.050	112.450	112.850	113.250
113.650	114.050	114.450	114.850	115.250	115.650
116.050	116.450				

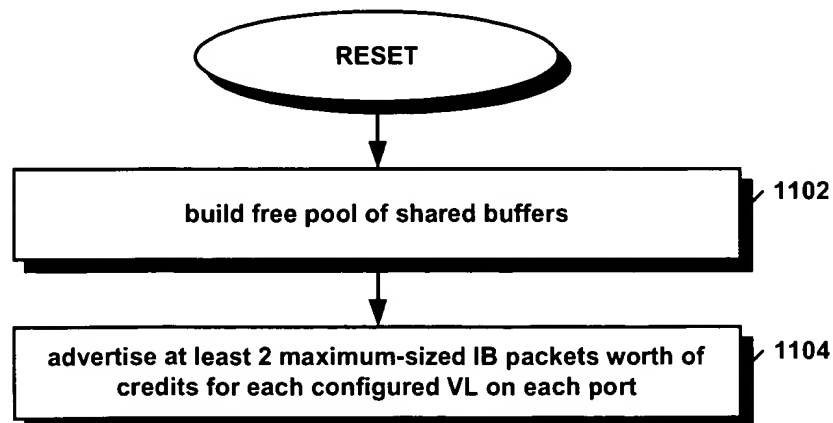
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FIG. 10



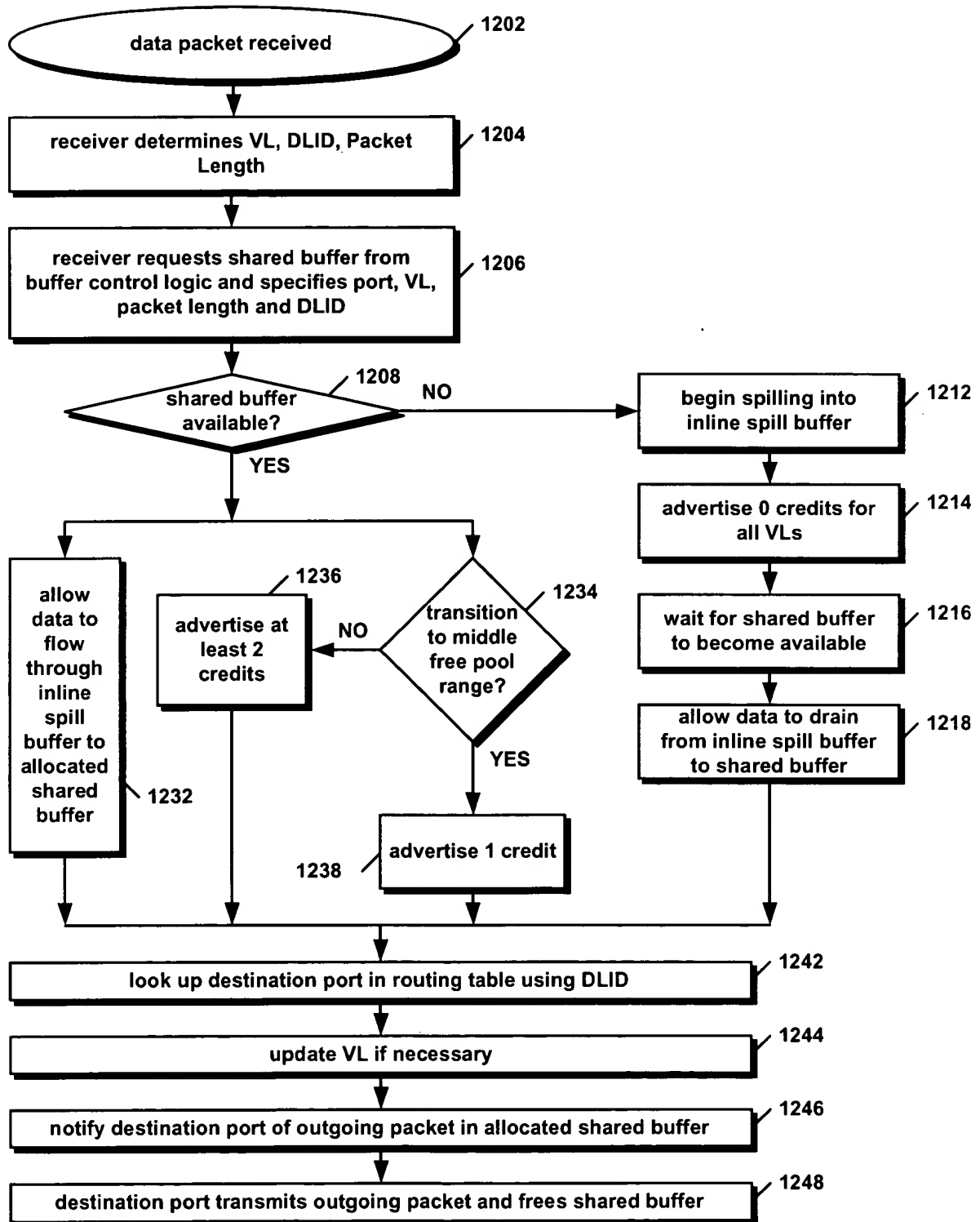
Timing Diagram For Determining Shutdown Latency

FIG. 11



Initialization

FIG. 12



Over-Advertising Flow Control

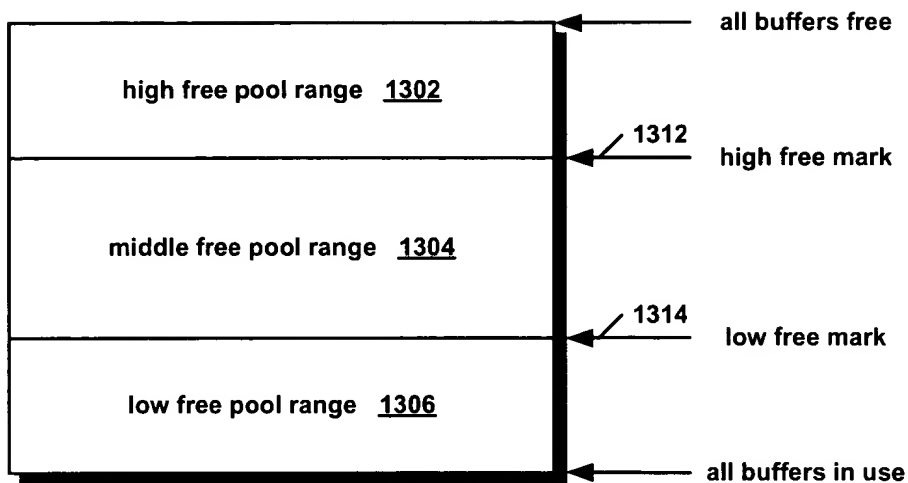


FIG. 13

Shared Buffer Free Pool Ranges

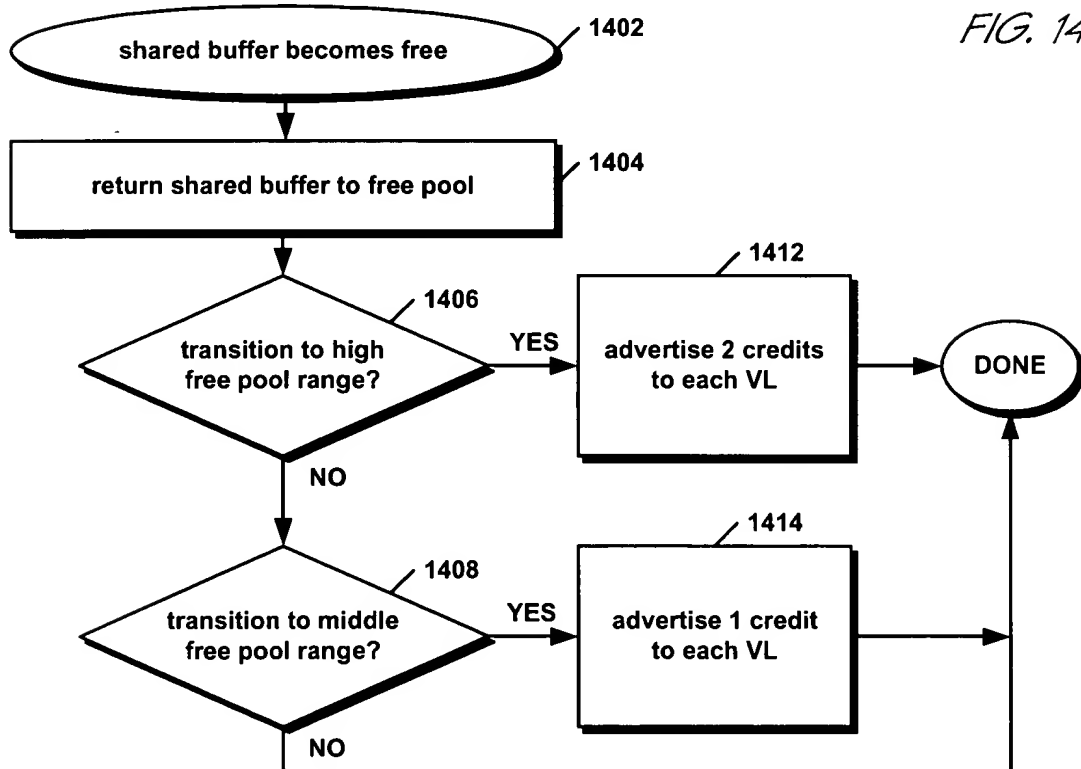
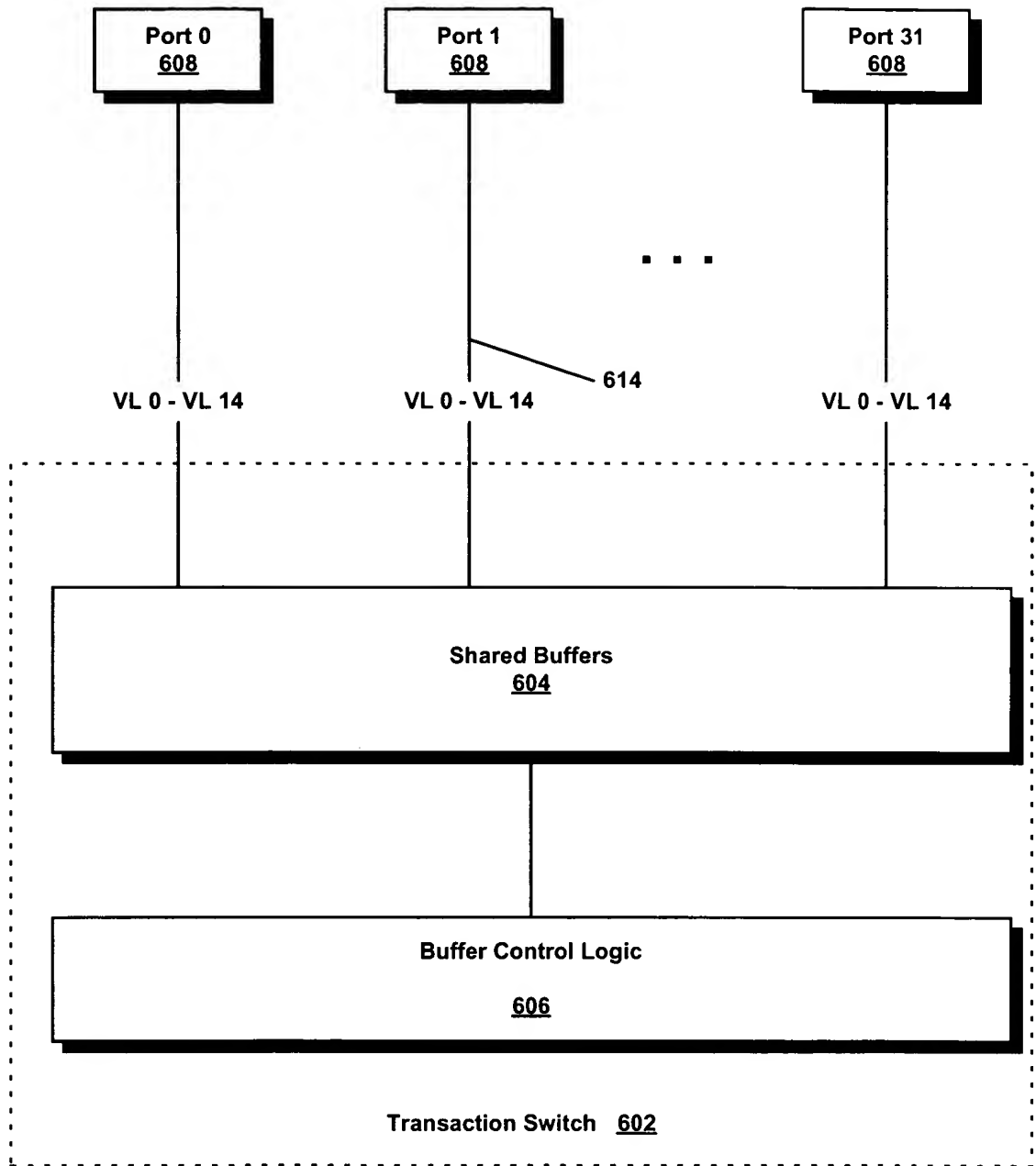


FIG. 14

Shared Buffer Free Action

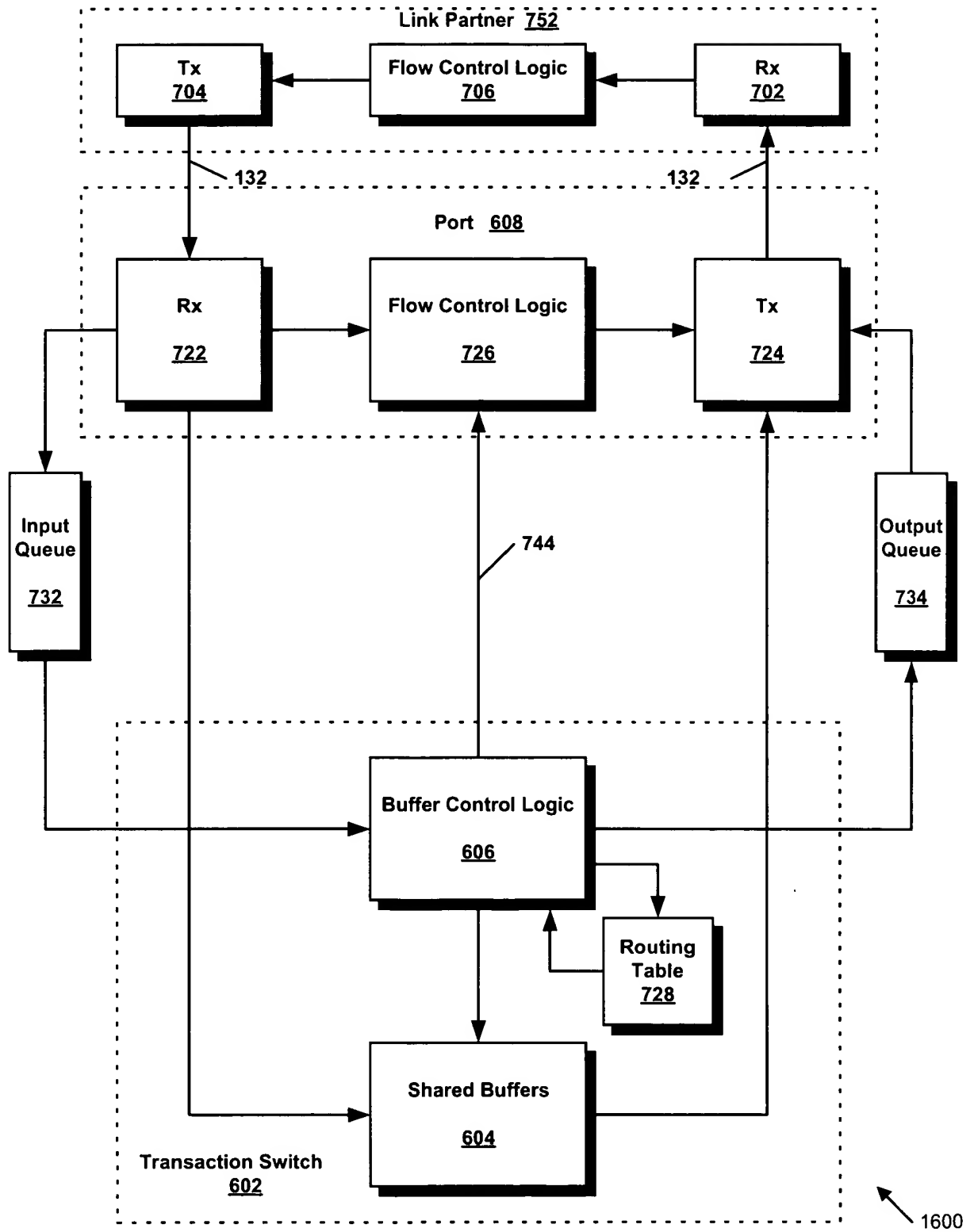
FIG. 15



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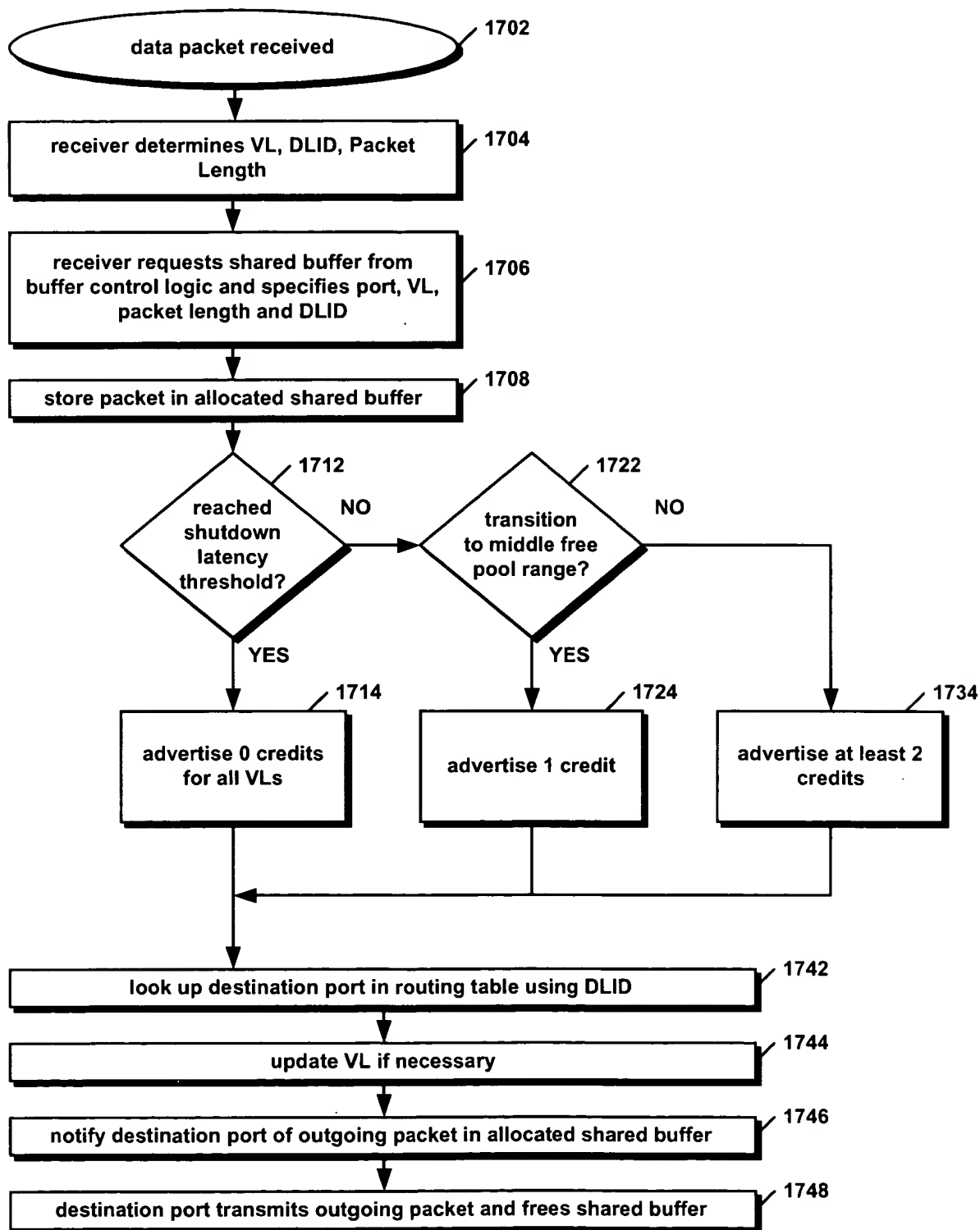
IB Switch Capable of Over-Advertising Buffering Resources Without Inline Spill Buffer

FIG. 16



Packet Buffering System Without Inline Spill Buffer

FIG. 17



Over-Advertising Flow Control

